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	Application No.	Applicant(s)
A	10/508,879	KRASIN, ALEXANDER
Notice of Allowability	Examiner	Art Unit
	Zeev Kitov	2836
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>08/17/06</u> .		
2. The allowed claim(s) is/are <u>1 - 6</u> .		·
 Acknowledgment is made of a claim for foreign priority unally All b) Some* c) None of the: Certified copies of the priority documents have Certified copies of the priority documents have Copies of the certified copies of the priority documents have and the priority	e been received. e been received in Application No cuments have been received in this r of this communication to file a reply of	national stage application from the
4. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which give	itted. Note the attached EXAMINER'	S AMENDMENT or NOTICE OF tion is deficient.
CORRECTED DRAWINGS (as "replacement sheets") must (a) ☐ including changes required by the Notice of Draftspers 1) ☐ hereto or 2) ☐ to Paper No./Mail Date (b) ☐ including changes required by the attached Examiner's Paper No./Mail Date Identifying indicia such as the application number (see 37 CER 1).	son's Patent Drawing Review (PTO-9 s Amendment / Comment or in the O	ffice action of
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).		
DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT	sit of BIOLOGICAL MATERIAL m FOR THE DEPOSIT OF BIOLOGICA	nust be submitted. Note the AL MATERIAL.
Attachment(s) 1. ☐ Notice of References Cited (PTO-892)	5. ☐ Notice of Informal Pa	atent Application
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Summary	(PTO-413),
3. ⊠ Information Disclosure Statements (PTO/SB/08),	Paper No./Mail Date 7. Examiner's Amendm	e nent/Comment
Paper No./Mail Date <u>08/17/06</u> 4. Examiner's Comment Regarding Requirement for Deposit	_	
of Biological Material		nt of Reasons for Allowance

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DETAILED ACTION

Examiner acknowledges a submission of the amendment and arguments filed on August 21, 2006. Claims 1 - 4 and 6 are amended. Amendment and arguments have overcome objections and rejections under 112, 2nd paragraph and 103(a).

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

An amended independent Claim 1 discloses an ESD protection circuit, which inter alia, includes a first and an NMOSFET and PMOSFET capacitors, wherein the PMOSFET capacitor is having a gate connected to the input node of the inverter, a drain and a source of the PMOSFET capacitor being connected to the ground rail, and a bulk of the PMOSFET capacitor being connected to the power rail.

The closest reference for the claim is Kerr et al., which discloses the PMOSFET capacitor (48 in Fig. 12) having a gate connected to the input node of the inverter (28 and 30 in Fig. 12) and a bulk of the PMOSFET capacitor being connected to the power rail. However, it does not disclose the PMOSFET capacitor having its drain and source simultaneously connected to the ground rail; the drain and source of the PMOSFET capacitor in the reference are left floating.

Another close reference is Stata et al. (US 5,825,601), which discloses the PMOSFET capacitor (MP2 in Fig. 3) having a gate connected to the input node of the inverter (MP3, MP1, MN1 in Fig. 3), while its source and drain are connected to the power rail (12 in Fig. 3). However, the connection of the PMOSFET bulk is not disclosed

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and therefore it is assumed as being connected as usually to the source of the transistor.

In contrast, the PMOSFET capacitor of the invention is being connected between the inverter input and the ground and is being controlled by the voltage between the power rail and the ground.

Allowability resides, at least in part, in the above-described limitations, which has not been disclosed in the Prior Art in a search.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (571) 272-2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (571) 273-8300 for all communications.

Z.K. 9/10/2006

> BRIAN SIRCUS SUPERVISORY PATENT EXAMINER

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